Received: October 19, 2021. Revised: December 28, 2021. 12

International Journal of
Intelligent Engineering & Systems

http://www.inass.org/

Design and Analysis of Improved 3-Stage LNA Architecture for CMOS RF Front End Receiver Systems

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Abstract: The development of high-performance Radio Frequency (RF) receivers requires an innovative RF front-end design to ensure the best performance out of good technology. Recently, in the industry of wireless technology, the production of receiver designs with better efficiency and performance is increased. A Low Noise Amplifier (LNA) plays a vital role in the performance of an RF receiver. LNA is most commonly designed with the increased number of stages which renders high gain by conquering the noise in the subsequent stages. The previous LNA design topologies (single-stage and two-stage) offer minimum Noise Figure (NF) and high voltage gain with increased power consumption and dissipation. The standalone parameter 'linearity' is indirectly dependent on power and it is clear that to achieve high linearity more quantity of power is required. In this research work, an improved three-Stage LNA with Cascode Topology (3S-LNA-CT) is designed with efficiency by satisfying the requirements like minimum NF, improved linearity, low power and high voltage gain. The proposed LNA architecture is realized using three stages in cascade connection because, in the receiver design, low noise and improved performance are the prior design constraints. Cadence Virtuoso software is used to implement the proposed three stage LNA design in 45nm Complimentary Metal Oxide Semiconductor (CMOS) technology. At end of the simulation, the 3S-LNA-CT design achieved 0.33 dB of NF, 7.92µW of power consumption, S11 and S22 values are evaluated -11.36dB and -17.54 dB respectively. The simulation performances of the 3S-LNA-CT is improved compared to the conventional LNA design such as Noise Cancelation Technique (NCT) LNA, Ultra-Wide Band (UWB) LNA, and Particle Swam Optimization (PSO) LNA.

Keywords: Cadence virtuoso, CMOS technology, Linearity, Low noise amplifier, Noise figure, Power.

1. Introduction

In recent years, modern wireless communication systems play a key role in day-to-day life which creates the demand for higher performance in terms of speed and mobility. The emerging mobile communication standards use different modulation techniques and different operating frequencies that would further explosively push the growth in the communication domain. Especially for the next evolution of technology, a high data rate with minimum signal interference is mandatory. LNA has become an important section in almost all RF and microwave receivers as it amplifies the weak signals without degrading the Signal to Noise Ratio (SNR). Designing an LNA with satisfactory performance aspects such as high gain, low signal interference, NF, and wide bandwidth is quite challenging. To resolve these challenges, a wideband co-design approach [1] of an active antenna with LNA at receiver level was designed but still, linearity improvement in the LNA design is not up to the level. In [2] Modified Derivative Superposition (MDS) technique improved the linearity of cascaded structure LNA and made it suitable for UWB applications. Various well-known techniques are used to design wideband LNA to significantly improve the gain and to reduce the NF at high frequency, power consumption and utilized area. Due to recent advancements, in the Band Width (BW) extension, it is necessary to combine the positive feedback cross-coupled capacitor with the

Active Inductor (AI) [3, 4]. For broadband applications, input second-order intercept point (IIP2) and input third-order intercept points (IIP3) are important. With the use of the Port Distortion Star Feedback (PDSF) [5] technique, intercept points (IIP3 and IIP2) are improved for a wide range of frequency which subsequently eliminates the harmonic and relatively causes high NF. To decrease NF in wideband LNA, the modification method in [6] analyses the input matching behavior in topologies like inductive degeneration, resistive and dual feedback to achieve the desired NF.

For different applications, LNA structure differs and in [7] the cascaded LNA design using stub matching network improved the gain and NF only at narrowband, which in turn for wideband linearity and gain gets deteriorated. In comparison with a stub, matching implemented cascaded LNA design the research [8] adopts a single cascade topology with resistive shunt feedback and an emitter degenerate resistor to provide a promising improvement in linearity characterized by the gain compression point. Furthermore, in [9-12] current reusing techniques have been widely used in a quasi-differential and linear configuration. The current biasing stream in the dc path reduces current consumption with biased current reuse and miller effect. While in ac path it provides a decoupling interaction between the stages that tend to increase the amplification level, stability and gain. For the 5G cellular RF front end receiver, techniques like Secured Socket Layer (SSL), SSL parallel series network [13] are incorporated in the LNA design. Further in [14, 15] multistage LNA that uses different topologies like cascade and cascode are introduced for high amplification and improved performance. But these techniques failed to achieve a perfect matched network because the return loss of the signal tends to be unsatisfied at both the ports.

As considering the issues in the prior existing works, this research paper presents an improved LNA design with multistage to improve the overall performance of the design and to provide high amplification for the RF receivers. The proposed design contributes some major points which are discussed below,

- The proposed 3-stage LNA design achieves high amplification of the signal so that the signal strength is not attenuated and provides good amplification for the signal.
- In this LNA design, cascading topology has been introduced to reduce the reverse isolation (S_{12}) and improves the stability of amplifier.
- A key feature of this design is that it reduces miller effect by suppressing the miller capacitance and improves the operating frequency of the amplifier.
- Additionally, the input/output reflection loss (S_{11} /S_{22}) is minimized, so the amount of signal lost is said to minimum.
- Further, this paper designs the LNA with minimum NF and better SNR ratio which makes the amplifier design to effective as it reduces the noise in the signal and improves the amplification.

The organization of this research paper is detailed as follows: Section 2 describes the related works of existing methods. Problem statements are elaborated in Section 3. In Section 4, the proposed three stage LNA circuit model I explained with the circuit diagram. The simulation results and comparison of the proposed design model with existing designs are explained in Section 5. Finally, Section 6 provides the conclusion of this research paper.

2. Related works

Caglar and Berke Yelten [16] developed a 180 nm CMOS X-band LNA structure that was operated under two cryogenic temperatures of about 77 K and 300K. In the proposed cascode LNA structure topology, linearity variations depend on cryogenic temperatures. The design was implemented in 180 nm technology that resulted in obtaining a moderate gain of about 18dB, 78 K noise temperature, and -3 dBm IIP3 as well as achieved better performance in linearity. For larger bandwidth, LNA's overall performance was degraded due to thermal noise and also results in a reduction of voltage gain.

Manish Kumar and Vinay Kumar Deolia [17] presented a low power LNA using Particle Swam Optimization (PSO) suitable for wide band applications. The main objective of this paper was to achieve low power, noise figure and wideband matching to improve the bandwidth. In this paper, two stages were introduced in the LNA design and PSO algorithm was employed to optimize the passive component parameters. The current reuse topology was the first stage where the combination of stacked P-channel Metal Oxide Semiconductor (PMOS) transistor on the N-channel Metal Oxide Semiconductor (NMOS) had been used with the series inductive peaking in the feedback loop to achieve better power results. Meanwhile, the mutually coupled Common Source (CS) stage was opted as second stage which used wideband matching to enhance the bandwidth and noise figure. The simulation results proven that it achieved S_{11} (<-10.9 dB), NF (2.4 dB) and power of about 1.6 mW. Though it achieved satisfactory results, it failed to

improve the reverse isolation S_{12} due to the miller capacitance.

Mahesh Mudavath [18] proposed an inductorless CMOS Low Noise Amplifier design with Noise Cancellation Technique (NCT) for wireless applications. In this proposed work, noise cancellation technique was adopted in the LNA design which contains Common Source (CS) and Common Gate (CG) amplifier stages. The phase mismatch issue was also taken into consideration and the LNA was designed effectively in 45nm CMOS processing technology. The simulation results within 1.04-1.8 GHz was obtained where the proposed design achieved minimum NF of 1.2 dB at 1.04 GHz, 0.6dB at 1.8 GHz and maximum gain of 20dB at 1.04 GHz, 23 dB at 1.8 GHZ. Due to centre biasing, the proposed design sensitivity was low for process and temperature variations with satisfactory linearity and 10% voltage fluctuation.

Mahesh Mudavath and Hari Kishore [19] presented a RF front end design of Inductor less CMOS LNA circuit with noise cancellation Method (NCM) for IoT applications. This paper focused on two paths parallely (i.e Common Source (CS) and Common Gate (CG)) where CS path was effectively designed to provide adequate gain and CG path improved input/output matching. The results examined that The CS path improved the gain of about 22.5 dB and CG path attained perfect matching network 50Ω. Moreover, it also attained minimum NF of 1.9 dB and input output return loss (i.e S_{11} and S_{22}) of -12.5 dB and -11.3 dB. For larger bandwidth, LNA's overall performance was degraded due to thermal noise and employed a reduction in voltage gain.

Mudavath [20] designed and analyzed the CMOS RF front-end receiver with optimized LNA and made it suitable for UltraWide Band wireless (UWB) applications. Receiver sensitivity depended on two foremost parameters namely NF and LNA's gain. In the proposed architecture two predominant LNA structures were designed and realized as single and two-stage LNA. It was concluded that two-stage LNA achieved a minimum NF of 0.9 dB, the high voltage gains of 32.5 dB and also reduced input-output return loss coefficients to create a perfectly matched network. Even though the necessary criteria were satisfied, the increase in power dissipation became an obstacle in achieving better linearity.

3. Problem statement

Problems associated with designing an efficient low noise LNA for RF front-end receiver are stated in this section followed by the explanations of how the proposed method overcomes the problems that were faced in the previous LNA designs. Designing an efficient LNA by satisfying all the design constraints is a complicated task. LNA is the main component in the receiver block and the issues faced in designing LNA are mentioned as follows:

- Some internal harmonics and thermal noise are introduced that cause increase in power dissipation [20] which affects the linearity.
- To achieve high linearity, the maximum amount of power is consumed by the source [20].
- NF parameter is degraded due to high voltage swing [17], improper SNR ratio and voltage gain also deteriorate with the continuous voltage fluctuations [19].
- For larger bandwidth applications receiver sensitivity and stability get affected [18].
- It is highly sensitive to flicker noise and DC offsets.
- A feedback network is introduced to improve the stability where active feedback introduces some noise which may significantly degrade the NF.

3.1 Solution

The implementation of three-stage LNA cancels the unwanted noise, TX leakage and due to the three consecutive stages, the internally generated harmonics are eliminated and the signal becomes a boosted signal without any distortion. This cascaded structure can be used for larger bandwidth applications and also due to the adoption of an improved suppression method, the voltage swing is minimized to obtain an effective NF, voltage gain and better linearity.

4. Proposed 3S-LNA-CT design

The fundamental component of the RF front-end receiver is a LNA. The key factors in designing a low noise amplifier are improved performance with low NF, high gain and improved linearity. In the proposed method, a three-stage LNA is designed to meet the requirements of design constraints. The proposed LNA is designed with the help of single-stage and two-stage LNA architecture.

4.1 LNA overview

LNA's role is important in the receiver chain of the wireless front-end systems as its main function is to amplify the weak signals and to maintain the proper SNR ratio. For the perfect case condition, SNR_{out} is equal to SNR_{in} but in real-world scenarios,

$SNR_{out}$is not equal to SNR_{in}. Since some amplifier noises are introduced by the active and passive components in LNA, these get amplified at the same rate causing the SNR_{out} to decrease. For that reason, LNA must be designed with minimum amplifier noise to keep the SNR_{out} high; otherwise the signal strength of SNR_{out} decreases then the signal will get mixed with noise and the data will be lost. While in most of the prior works Common Source (CS) LNA uses single and multi-transistor based topologies. Some of the issues faced in CS LNA are stated below,

1. Reduced bandwidth due to high load.
2. Low electrical stability.
3. Low output impedance zo.
4. Low reverse isolation S_{12} due to g_d connecting in out.

The aforementioned issues of CS LNA are overcome by changing the designing topology because topology selection is considered to be very important in the design of LNA. In the proposed 3 stage cascode LNA architecture the aforementioned shortcomings are rectified which was not possible in the prior existing works. In this paper, the most widely used cascode topology is used to design the LNA architecture.

4.2 Three-stage LNA:

In the single and two-stage LNA architecture, power dissipation is increased due to the internally generated harmonics and thermal noise. This significantly reduces the linearity which is one of the important criteria in designing an LNA and this further creates problems in the receiver's performance. To overcome these problems, three-stage LNA architecture is proposed in this method. The proposed design contains 3 stages to strengthen the signal for additional processing and to remove the unwanted harmonics and cancel the distortion in the signal. Three-stage LNA is designed by cascading the two-stage LNA architecture with single-stage LNA, where the output of the two-stage LNA acts as input to the next succeeding stage. In this cascaded architecture, the weak signal from the antenna source is passed through stage by stage. Design considerations like minimum NF, high voltage gain, power gain and improved linearity are satisfied in the three-stage LNA architecture to produce a better performance in the RF front-end receiver.

4.3 Cascode topology

In the common source topology another transistor is introduced (i.e. cascode transistor) which is employed as an output buffer. This helps to improve the performance of the LNA.

Cascode transistor is designed to have voltage (and power) gain using the below mentioned Eqs. (1) to (3).

$$v_{in} = -v_{gs} = \frac{i_{in}}{jwC_{gs}+g_m} \tag{1}$$

$$v_{out} = -g_m v_{gs} Z_L = \frac{i_{in} g_m Z_L}{jwC_{gs}+g_m} \tag{2}$$

$$A_v = \frac{v_{out}}{v_{in}} = g_m Z_L \tag{3}$$

Where, V_{out} = output voltage, V_{in}= input voltage, V_{gs} = gate to source voltage, i_{in}= input current, g_m = transconductance, Z_L = load impedance and A_v = voltage gain.

4.4 3S-LNA-CT circuit operation

The improved 3 stage LNA architecture is proposed for all kinds of receivers in the communication systems. In this architecture, 3 stages have been introduced to improve the overall performance of LNA. Before designing any multistage amplifier, the very important factors to be considered are: the single stage amplifier has to be properly designed with accurate values of the components and a well-suited topology must be chosen based on the requirement. In this proposed paper, the single stage LNA is designed based on the cascode topology with inductive source degeneration. It contains 4 internal circuits that include the input impedance matching circuit, Common Source stage (CS), Common Gate stage (CG), and the output matching circuit. Meanwhile, the next consecutive stages are designed by recursively connecting the single-stage LNA at their respective output. The schematic diagram of the 3 stages LNA is shown in Fig. 1. It requires '6' nMOSFFET transistors in which NM0 and NM1 are for the first stage, NM2 and NM3 are for the second stage and finally, NM4 and NM5 are for the third stage. The input and output matching circuitry require some lumped components such as a resistor, capacitor and inductor. In this schematic design, input matching circuitry consists of inductor $1 = 350p$, capacitor $C1 = 4pF$, $C2 = 3pF$, $C3 = 5pF$ and resistor $R1 = 5K\Omega$ that are utilized to obtain the suitable value of input reflection co-efficient (S_{11}) at 5 GHz centre frequency. The input signal flows through the gates of the transistors NM1 and NM0 where reference voltage $V_{ref}$is fixed at the gate of NM0 using elements like inductor $L3 = 5nH$, $L4 = 12nH$, capacitors $C4 = 1pF$, $C5 = 1pF$ and

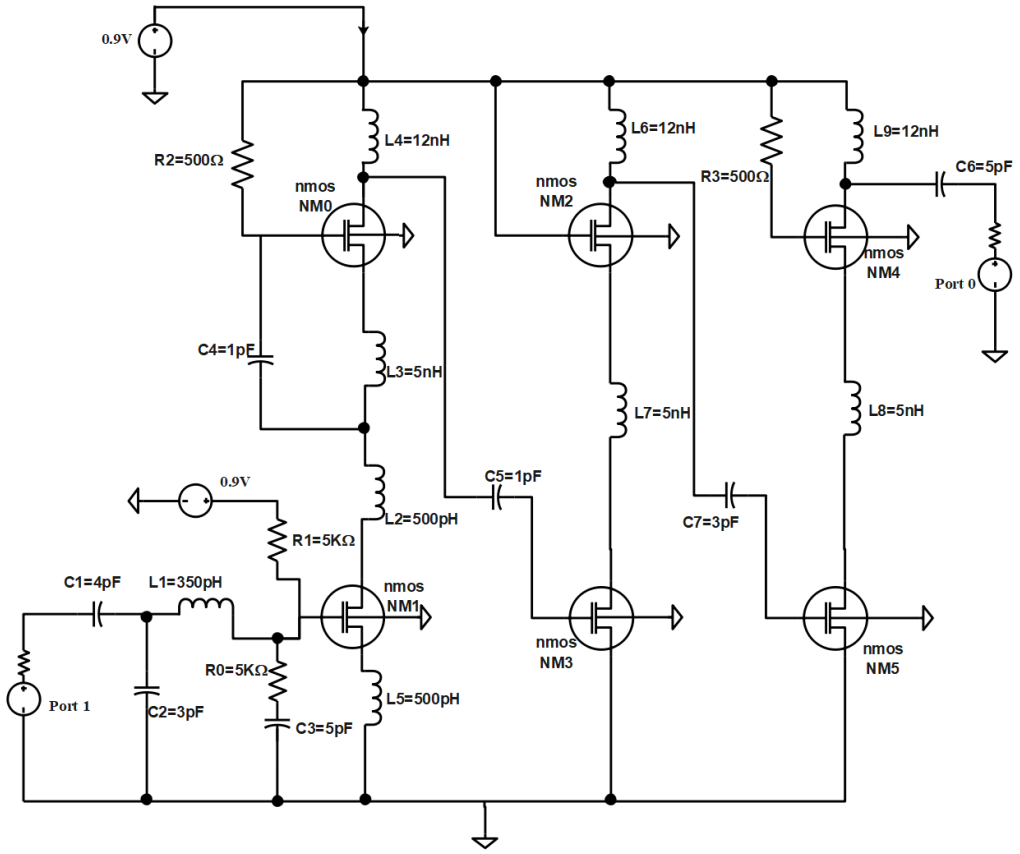

Figure. 1 Schematic diagram of the 3 stage LNA architecture

resistor $R2 = 500\Omega$. so that both the transistors NM0, NM1 operate in the saturation region. Moreover, M0 and M1 transistor width and length is represented as 120nm and 45nm respectively. Similarly, M2, M3, M4, and M5 transistor width and length is represented as 45nm and 240nm respectively. As mentioned early in the section 4.1, that the proposed architecture uses cascode topology, here the lower transistor NM1 works in common source configuration while the upper transistor is the cascode transistor that works in common gate configuration which is employed to act as a buffer and to isolate the output node from input.

The cascoding transistor reduces the interaction of gate-drain capacitance of NM1and its presence renders the input and output matching networks which are independent of each other. Furthermore, NM0 suppresses miller capacitance which results in improved reverse isolation (S_{12}). Due to the suppression of the capacitance of the input transistor, the NM1 transistor helps in improving the operating frequency of the amplifier. To improve the flexibility and to reduce the scope of possibilities, the gate of the transistor NM0 is assigned a maximum voltage. Additionally, inductor $L2 = 500pH$ acts as series peaking inductor between input and output to enhance gain and bandwidth, whereas due to the inductor Ls, improvement in the stability of the amplifier is observed. For high gain amplification, the further next two stages are connected in cascade fashion without violating the design considerations as all the amplifiers are matched to 50Ω. The output signal of the NM0 is again passed to the input transistor NM3 of the next level with the gate capacitance of about $C5 = 1pF$. Similar to the previous stage, here also NM2 acts as the cascode transistor where inductor $L7 = 5nH$, and $L6 = 12nH$, fix the V_{ref} at the gate of the transistor NM2. Besides, the output signal of the NM2 surpasses the third stage input transistorNM5with gate capacitance $C7 = 3pF$ where NM4 acts as a cascode transistor which acts like a buffer and isolates the output node from input and the same operation in previous stage is repeated. Finally, the output matching circuit provides output impedance matching and the signal strength is boosted effectively with the recursive amplification in the design. Thus the proposed design offers high gain due to the increase in output impedance and improves the bandwidth, electrical stability and reverse isolation is reduced. The brief explanation of the performance parameters and their relations with each other in the 3 stage LNA design, is stated below.

4.4.1. Stability

The correct functionality of the 3 stages of LNA is determined with the help of this critical parameter. In this 3 stage, LNA the most commonly preferred methodology to check the stability is a calculation of the Rollett stability factor (K-factor), using the S-parameters of the proposed LNA, as shown in Eqs. (4) and (5). This method helps to ensure the stability of the amplifier over a wide range of frequencies.

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}\,S_{21}|} \quad (4)$$

Where

$$\Delta = S_{11}\,S_{22} - S_{12}\,S_{21} \quad (5)$$

When K>1K>1and $|\Delta| < 1|$ then the LNA is said to be unconditionally stable, if $K<1$ and $|\Delta|>1$ means the stability of the LNA gets affected. Therefore, the designed 3 stage LNA is unconditionally stable regardless of the frequency of its operation.

4.4.2. S-parameters

S-parameters are also very important for the LNA design wherein parameters like input S_{11}, output S_{22} reflection coefficients, gain S_{21} and reverse isolation S_{12} are calculated using the S-parameter two-port network. The input and output reflection coefficients prove how the 3-stage LNA is matched to source and load impedance (50Ω) at different frequency bands. Whereas the reverse isolation S_{12} measures the isolation of the input and output ports which are being improved in the 3 stage LNA design. However, Gain is being expressed with S_{21} in scalar logarithmic unit (dB) and the calculation is done using the below Eq. (6).

$$g = 20\log|S_{21}|dB \quad (6)$$

4.4.3. Noise figure

Noise Figure measures the amount of degradation of the signal to noise ratio in between the input/output ports of the proposed LNA design and it is expressed as in Eq. (7).

$$F = \frac{S_i/N_i}{S_o/N_o} \quad (7)$$

Where Si, Ni denotes the input signal and noise power respectively and So, No denote the output signal and noise power respectively.

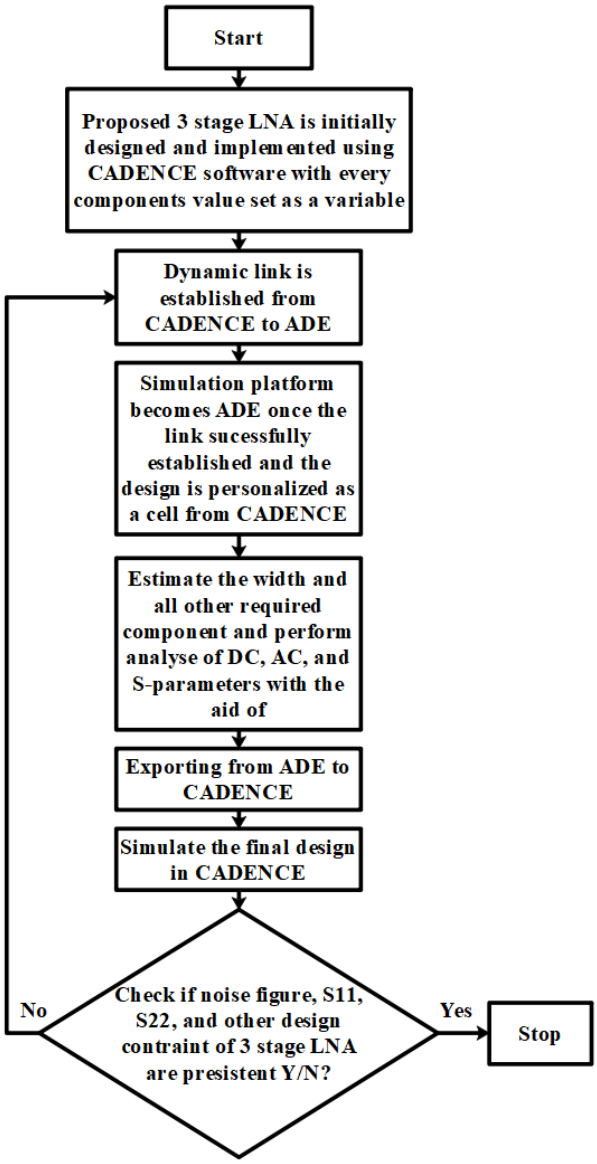

Figure. 2 Flow chart of the overall simulation flow

It is clearly stated in this equation that the NF tends to increase with the trade-off between the input and output SNR ratio. For the proposed 3 stages LNA, the NF is calculated using the Friis formula which is given in Eq. (8).

$$F_{total} = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_2} \quad (8)$$

Certainly in the proposed design 3 stages are incorporated so the NF equation is also altered according to that. Where F_{total} measures the overall NF of the design whereas F_1, F_2, F_3, G_1, G_2 and G_3 are NFs and gain of the first, second and third stages respectively. It is clear from Eq. 8 that the NF of the first stage dominates the noise performance of the remaining two stages. Therefore, in the proposed design, the architecture of the first stage is optimized

for low possible NFs and to produce excellent NF performance in the overall system.

Finally, the 3 stage LNA is designed and simulated using the Cadence Virtuoso 45nm technology. The entire simulation flow is stated in the below flowchart of Fig. 2.

Initially, the 3 stage amplifier circuit is designed using PMOS, NMOS transistors, and (Resistor – Inductor - Capacitor) RLC components. After designing the LNA, the dc, ac and s parameter analysis have been simulated using cadence software. With the help of these analysis, the performance parameters such as NF, S_{11}, S_{22} parameter, stability factor and power consumption are improved in 3S-LNA-CT design compared to the conventional designs.

5. Simulation setup

The proposed design was implemented using the following system requirements: 8GB RAM with 1.6GHz of speed and 1TB hard disk. Cadence Virtuoso is the most commonly used software because of its unique attribute i.e., it creates an integrated methodology that automates and reorganizes the design and verification flow for various heterogeneous systems. The proposed 3 stages LNA was designed and simulated using Cadence Virtuoso and Analog Design Environment (ADE) software with 45nm technology. The simulation parameter of the proposed design is given in Table 1.

Table 1. Simulation parameter of proposed design

S. No.	Parameters	Values
1	Design	3 stage LNA
2	Analysis	DC, AC, SP
3	SP frequency	5 GHz
4	AC frequency	5 GHz
5	Port 0 and 1 resistance	50 ohm
6	Port 0 and 1 source type	Sine
7	Power Supply (PS)	0.9V
8	Area	54μm^2
9	Bias voltage	0.9v

5.1 Results and discussion

The simulation results and discussion of the 3 stages Low Noise Amplifier (LNA) are discussed in this section. The schematic in Fig. 6 is simulated using the Cadence Virtuoso and ADE software under 45nm processing technology. The following figures show the post-simulation results of the 3 stage LNA.

5.1.1. Input matching (S_{11})

The input reflection coefficient (S_{11}) of the designed 3 stage LNA should be less than -10dB while maintaining a low NF. In the designed cascode 3 stage LNA,-11.3657dB is achieved at 0.2GHz frequency which is shown in the below plot 3. The magnitude value (0.987) performed the $20log.100$ operation and generated the -11.3657dB results.

From the plot, it is certainly clear that the designed LNA achieves improved input matching since the reflection coefficient S_{11} (i.e. scattering parameter which measures the amount of reflection at port 1) is comparatively less and so the amount of reflection at the input port is improved, which subsequently reduces the input return loss.

Further for the S_{11} parameter, the smith chart plot is created, which represents the input reflection coefficient in the polar graph format. The smith chart representation of the S_{11} parameter is present in Fig. 4.

5.1.2. Output matching (S_{22})

The output reflection coefficient S_{22} of the designed LNA architecture is low since it has low output impedance, so the required output matching is attained without any output filter network at the

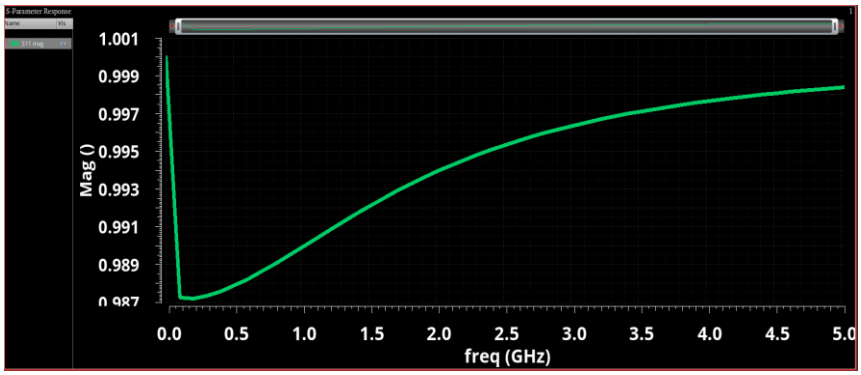

Figure. 3 Magnitude plot of S11 parameter

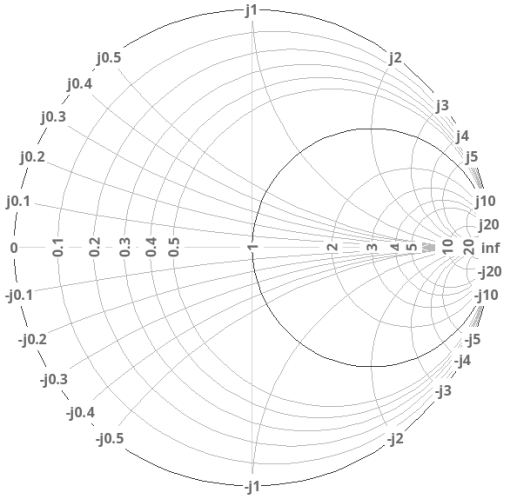

Figure. 4 Smith chart representation for S11 parameter

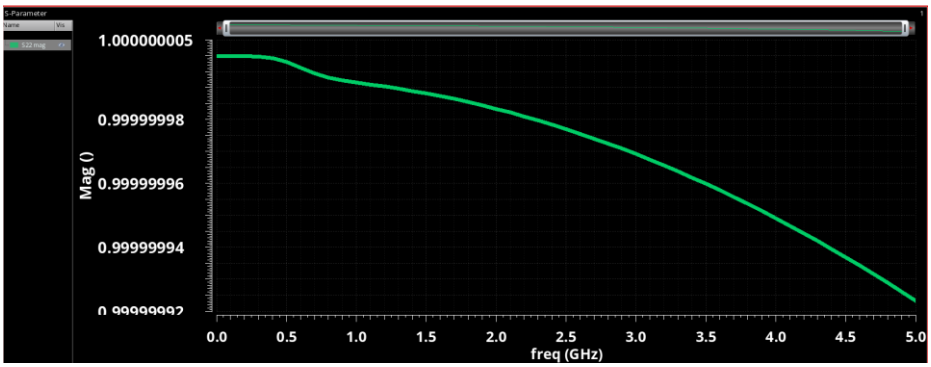

Figure. 5 Magnitude plot of S22 parameter

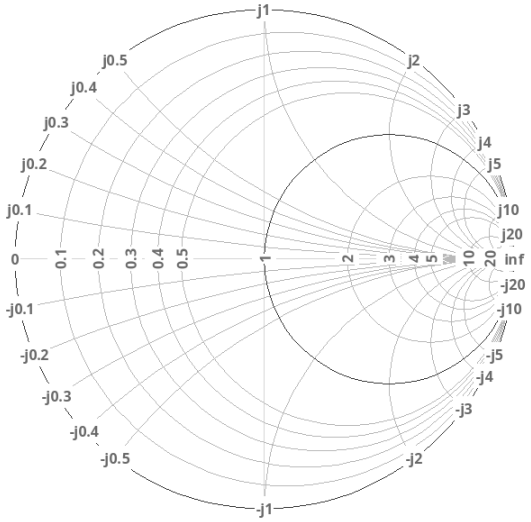

Figure. 6 Smith chart representation for S22 parameter

output port and it does not change the DC bias. The 3 stage cascode LNA design achieved -17.548dB at 0.2GHz of frequency which is shown in Fig. 5. The magnitude value (0.98) performed the $20log.100$ operation and generated -17.548dB results.

It is noted from the plot that the output reflection coefficient S_{22} (i.e. scattering parameter that measures the amount of reflection at port 2) is comparatively reduced so that the output return loss is minimized which helps in improving the performance of the design. The smith chart representation for S_{22} parameter is presented in Fig. 6.

5.1.3. Noise figure (NF)

The noise figure for the designed LNA is shown in Fig. 7 and 8. From the result, it is certainly proven that the designed LNA achieves a better NF of about 0.33dB. NF or noise factor measures the amount of degradation of the Signal-to-Noise ratio (SNR). If the SNR value is reduced, it significantly improves the NF which helps to increase the system performance. Hence, the designed LNA adds a very low amount of noise and it achieves a better SNR ratio since it has a low NF.

5.1.4. Stability factor and power

As previously stated, the stability is considered to be an important consideration in the LNA design that can be derived from S-parameters, the matching networks and termination. The stability factor for the designed LNA is calculated using the Rollett equation under the frequency band 0.425 GHz to

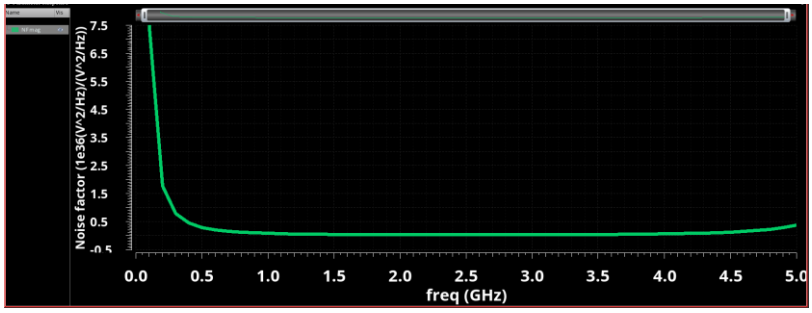

Figure. 7 Magnitude plot of NF

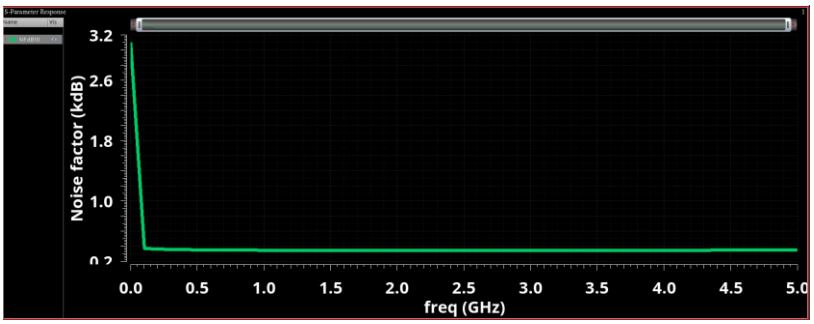

Figure. 8 Decibel plot of NF

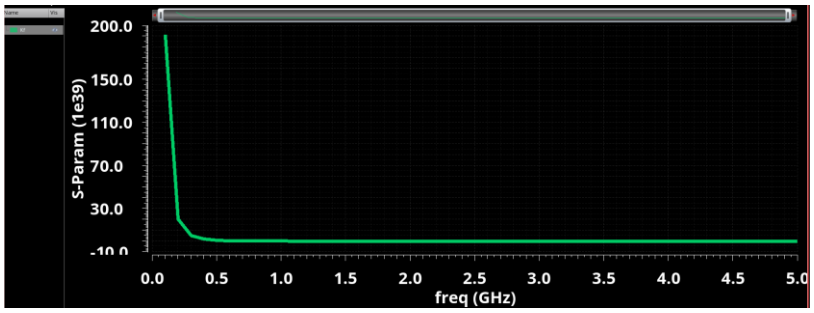

Figure. 9 Stability factor plot of 3 stage LNA

0.745 GHz. The designed 3 stage LNA attains improved unconditional stability greater than 1 at 0.7GHz as shown in Fig. 9.

While coming to the power results of the proposed 3 stage LNA, it consumes only 7.92µW of power. Due to the improved matching condition, both at the input and output port, the power loss is minimized which significantly improves the power consumption.

5.2 Performance analysis

In this section, the overall performance parameters of the 3 stage LNA obtained from various plots are discussed together. The overall performance metrics of the proposed 3 stage LNA are tabulated in Table 2.

In the above performance analysis table, parameters like NF, S_{11}, S_{22}, stability and power values are stated. It proves that the proposed design has a lower NF so the degradation of SNR ratio is minimized which maintains the unconditional stability. While coming to the input and output reflection coefficients (S_{11} and S_{22}), this designed LNA attains good values which indicate less amount losses at the input and output port. Due to the less amount of reflection, the signal attenuation is reduced and subsequently, it results in minimum power usage. Overall, the proposed low noise amplifier provides satisfactory performance values which makes it suitable for implementation in the receivers of the communication systems.

Table 2. Overall performance analysis of proposed design

S. No.	Performance parameters	Proposed 3 stage LNA
1	NF (dB)	0.33
2	S11 (dB)	-11.3657
3	S22 (dB)	-17.548
4	Stability	>1
5	Power (W)	7.92µW
6	Smith chart unity factor	1
7	Stability factor	190
8	Alternative stability factor	300

Table 3. Comparison table of various LNA designs with the proposed LNA

LNA Works	Design type = Experiment (E)or Simulation (S)	Technology	NF (dB)	S_{11} (dB)	S_{22}(dB)	Power	Gain (dB)	PS (V)	Frequency (GHz)
PSO-LNA [17]	S	45nm	2.4	<-10.9	NA	1.6mW	18.57	0.8	5-27.5
NCT-LNA [18]	S	45nm	1.2	-11.2	-12.8	-	20-23	1.2	1.04-1.8
INCM-LNA [19]	S	45nm	1.9	-12.5	-11.3	6.7mW	22	1.2	1.04
UWB - LNA[20]	S	45nm	0.9	-11.6	-10	11.8mW	28.8	1	3.4
Proposed 3S-LNA-CT	S	45nm	0.33	-11.3657	-17.548	7.92µW	31.24	0.9	10.5-32.1

5.3 Comparative analysis

The comparative analysis of the proposed 3 stage LNA design with the existing designs is described in this section. The proposed design is compared with the existing methods such as Gm boosted LNA, noise & distortion canceling LNA, Cascode CS LNA, Current reuse and Common Gate LNA design. The comparative analysis is taken in terms of NFs, S_{11}, S_{22} and power. Table 3 shows the comparison result of the proposed LNA with the aforementioned existing methods.

From Table 3, it is proved that the proposed LNA design achieves better results in terms of the aforementioned parametric measures. In the PSO-LNA work [17], the switch terminal act as a transmitter and receiver. This design model process with high isolation and effective gain. But, the linearity of the LNA was poor due to the more DC bias voltage. In NCT-LNA [18], the design model is processed with the average noise temperature. However, the circuit needs to be concentrated on the effective NF. Meanwhile comparing the next work of designing Inductor-less NCM (INCM) LNA [19], it attains minimum NF (1.9dB) but fails to improve the reverse isolation that tends to increase the power dissipation. In the UWB-LNA method [20] NF is considered satisfactory, where it only improves 0.9 dB of input reflection coefficient that in turn affects the power. On the account of increased input return loss, this design required 11.8mW of power. Finally, while comparing all the prior existing works it is distinctly proved that the proposed 3 stage LNA delivers improved results in all the evaluation parameters (i.e. NF 0.33dB, S_{11}=-11.3697dB, S_{22}=-17.548dB and power = 7.92µW) to a satisfiability extent and therefore it is a very effective LNA design for smooth implementation in the communication system. But, S_{11} parameter needs to be concentrated more to obtain the better results in the future. The PS, gain, and frequency of the proposed work also evaluated in this research work. The all the conventional designs results are taken from the literature papers and the respective results are tabulated.

6. Conclusion

In this paper, an efficient low noise amplifier with 3 stages is designed using cascode topology. The designed 3 stage cascode amplifier is successfully implemented and simulated using cadence virtuoso and ADE software, where results are compared with the other existing works which certainly proves that the 3S-LNA-CT design is eminently suitable for the receivers in a wireless communication system. Due to the incorporation of 3 stages, high amplification is achieved which in turn improves the performance. Furthermore, the signal strength is not attenuated (i.e. no reduction in signal strength) due to the proper input-output matching that consequently minimizes the power loss, and hence the data is not lost. Moreover, it improves the reverse isolation by reducing the miller capacitance. Overall this design exhibits great performance in terms of NF (0.33dB), unconditional stability (>1 at 0.7GHz), power (7.92µW) and reduced input/output return loss (S_{11}= -11.3657dB and S_{22}= -17.548dB) and satisfies the needs of the amplifier which is greatly used in the entire RF front end receiver. In the future, different compensatory circuit will be simulated and experimented in the three stage LNA design to improve the power consumption and NF. Moreover, the physical model of the circuit design will be implemented to improve the gain and frequency.

Conflicts of Interest

The authors declare no conflict of interest.

Author Contributions

The paper background work, conceptualization, methodology, dataset collection, implementation, result analysis and comparison, preparing and editing draft, visualization have been done by first author. The supervision, review of work and project administration, have been done by second author.

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